Concept

OVERVIEW

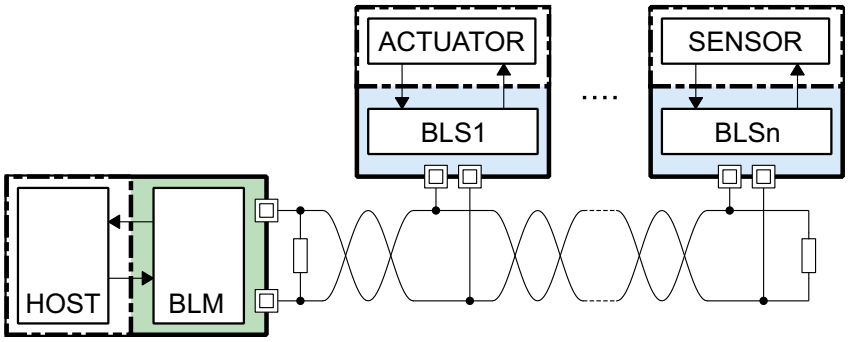

Figure 1: BiSS Line topology with one *BiSS Line* Master (BLM) and at least one *BiSS Line* Slave (BLS)

BiSS Line is a one-cable technology based on *BiSS Interface* (**Bi**directional/**S**erial/**S**ynchronous). It enables a fast, isochronous and robust bidirectional data transmission between a *BiSS Line* Master (BLM) and at least one *BiSS Line* Slave (BLS). *BiSS Line* is typically used in motion control applications to transmit data from BLM to a BLS (e.g. actuator data) and data from BLS to the BLM (e.g. sensor data) with low jitter. *BiSS Line* requires only two wires for a combined power and data transmission over transmission lines up to 100 m. The bus-capable data transmission is based on the industrial standard RS485 and protected by Forward Error Correction (FEC) against electromagnetic interference, e.g. induced from PWM signals to the data line. In a *BiSS Line* system with one sensor and a total data length of 48 bit (position data, status and CRC) transmitted over 100 m cable, cycle times well below 31.25 µs can be achieved.

BiSS LINE SYSTEM STRUCTURE

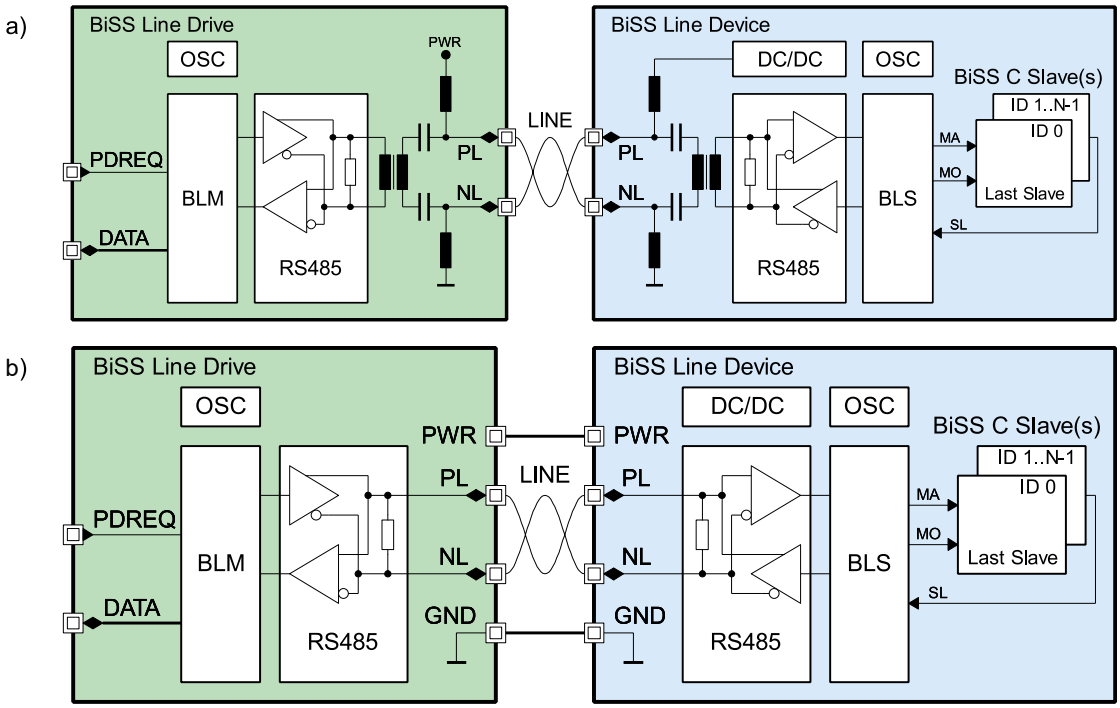

Figure 2: 2-wire configuration (a) and 4-wire configuration (b)

2-Wire Configuration
In order to reduce cabling, the 2-wire configuration is used. It requires coupling elements to modulate the data signals onto the power supply. The positive *BiSS Line* signal (PL) consists of the DC input voltage (PWR) and the data signal. The negative *BiSS Line* signal (NL) consists of the inverted data signal modulated onto ground voltage level. The differential data signal before modulation is RS485 compatible.

4-Wire Configuration
If there is not sufficient space for coupling elements as described for the 2-wire configuration, then data signals and power supply can be transmitted separately. The *BiSS Line* signals (PL, NL) consists of the differential data signal and are RS485 compatible. The DC supply voltage (PWR) and ground (GND) are connected via separate lines.

BiSS LINE FRAME OVERVIEW

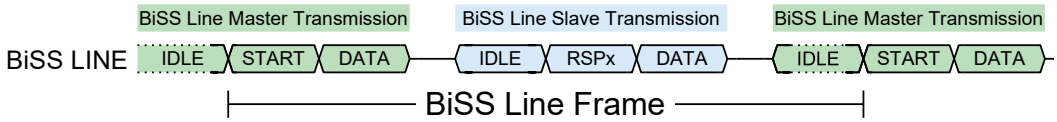

Figure 3: Frame with *BiSS Line* master request (green) and *BiSS Line* slave response (blue)

Introduction
The *BiSS Line* communication between one *BiSS Line* master (BLM) and at least one *BiSS Line* slave (BLS) is established with frames using a RS485 half-duplex serial transmission. *BiSS Line* uses a 8B10B coding to prevent charging of the transmission line. With the 8B10B coding, the fixed *BiSS Line* data transmission rate of 12.5 Mbit/s matches a typical sensor clock frequency of 10 MHz (e.g. of a BiSS C or SPI sensor) enabling a simple conversion between the protocols. A *BiSS Line* frame is initiated by the BLM and finished by a BLS. In between of the frames, the BLM sends an IDLE symbol. At the beginning of a frame, the BLM interrupts the IDLE symbol and sends one of two START symbols (REQ, AUX).

- REQ initiates a Process Data Frame (PDF),
- AUX initiates an Auxiliary Data Frame (ADF).

The START symbol is followed by DATA that depends on the initiated type of frame. When the BLM stops its DATA transmission, the BLS responses starting with an IDLE symbol, followed by one of two response symbols RSPx (RSP0, RSP1) and its DATA. Afterwards, the frame is completed and the BLM takes over again sending IDLE symbols until the next frame begins.

IDLE Symbol
The IDLE symbol is a stream with alternating high/low levels (1010...) suitable for clock recovery. The constant switching also prevents charging of the transmission line. The IDLE length is not determined and the BLM can abort the IDLE signal after any zero bit. A long IDLE signal helps the receiver to identify the phase of the *BiSS Line* signal even in disturbed environments.

START/RSPx Symbol
The two START symbols (REQ, AUX) and the two RSPx symbols (RSP0, RSP1) have been selected carefully in order to ensure detection of the beginning of the communication. Figure 4 shows the Hamming Distance between the received code, which is loaded into a 14 bit wide register, and a comparative value for START/RSPx detection. During IDLE and transmission of a START/RSPx symbol, the hamming distance is always five and above. At the moment when the START/RSPx symbol is received completely, the hamming distance becomes zero. This allows the receiver to reconstruct the end of the START/RSPx signal, even if one or two bits are flipped during transmission.

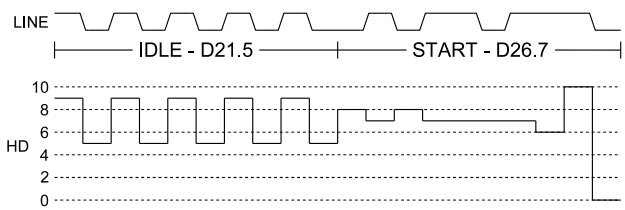

Figure 4: BiSS Line IDLE and START/RSPx symbol

PROCESS DATA FRAME (PDF)

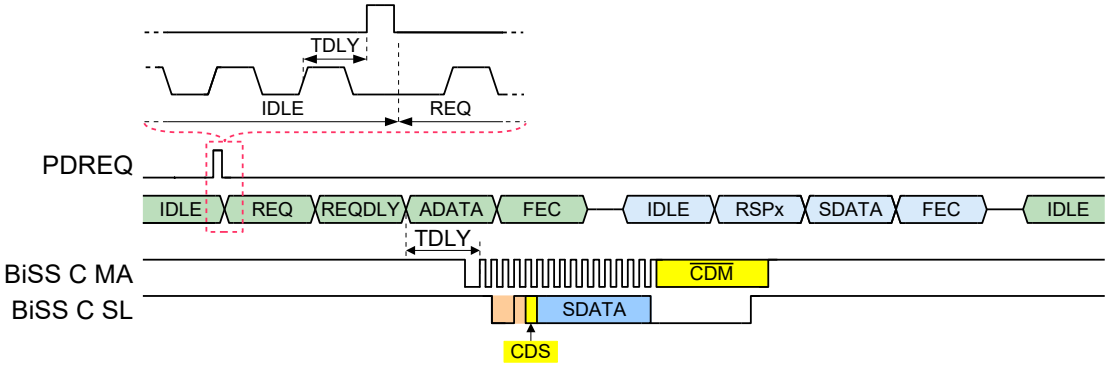

Figure 5: Process Data Frame (Example for BiSS C Sensor)

BiSS Line is particularly suitable for isochronous process data transmissions (e.g. in motor feedback systems). Data can be transmitted from master to slave (e.g. actuator data) or from slave to master (e.g. sensor data). The capturing of sensor data is triggered by a controller in the drive. Typically, the trigger event is asynchronous to the IDLE on the transmission line. *BiSS Line* minimizes the jitter between the process data request (PDREQ) from the controller and the latch event in the sensor. Therefore, after the start symbol for process data transmission REQ, the delay TDLY between the trigger event and a rising edge on the transmission line is measured and transmitted as part of the REQDLY symbol (Figure 5). When the *BiSS Line* slave receives REQDLY, it delays the sensor latch point by TDLY to ensure equidistant data acquisition.

Process Data

The process data, either actuator data (ADATA) or sensor data (SDATA), is transmitted as part of a logical data channel. Each data channel can contain additional data (e.g. status bits and CRC) and is transmitted completely in every PDF. The process data is 8B10B coded with the benefit of DC balance and sufficient transitions for clock recovery. A Forward Error Correction (FEC) is used to increase data availability and to reduce the error rate in disturbed environments. To ensure compatibility with *BiSS C*, Control Communication (e.g. register accesses) is performed within the Process Data Frame.

Control Communication

Control Communication has been introduced with *BiSS C* to enable access to the slave's memory without interrupting the process data transmission. Control Communication can be used to configure or calibrate sensors, transmit slowly changing sensor data (e.g. temperature) or to read an implemented electronic datasheet. To this end, one bit of Control Data is transmitted in each *BiSS C* frame from *BiSS C* master to slave (CDM) and from slave to master (CDS).
BiSS Line uses the same concept and exchanges one bit of control data in each Process Data Frame. The CDM bit is transmitted as part of the REQDLY symbol, while the slave's respond CDS determines which RSPx symbol is transmitted: CDS=0 $\Rightarrow$ RSP0, CDS=1 $\Rightarrow$ RSP1. The Control Data Bits of several PDF form a Control Data Frame with lower throughput compared to the process data transmission, for instance, a read access to a single register of a BiSS C slave requires 32 PDFs.

AUXILIARY DATA FRAME (ADF)

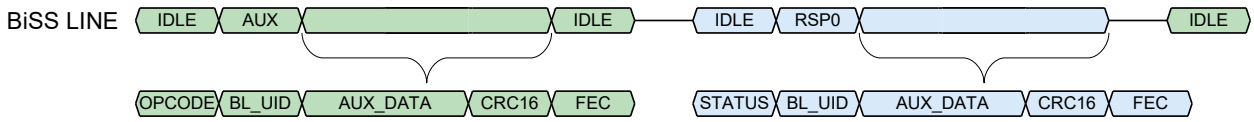

Figure 6: Auxiliary Data Frame

The Auxiliary Data Frame (ADF) enables fast register accesses to the *BiSS Line* slaves and implementation of advanced *BiSS Line* systems. It is used to establish bus topologies with more than one *BiSS Line* slave by assigning a time slot for process data transmission to each slave. The START symbol is followed by an OPCODE and addresses a specific *BiSS Line* slave using a unique *BiSS Line* ID (BL_UID). The transmitted AUX_DATA is protected by a 16 bit CRC and Forward Error Correction (FEC).