Concept

OVERVIEW

The open source BiSS Interface protocol implements a realtime interface for a digital, serial and secure communication between drive, sensor and actuator. It is used on the lower sensor/actuator communication level in industrial applications which require short cycle times, safety, flexibility and minimum implementation effort. In addition to its technical advantages, two characteristics have ensured the success of the open global standard: the free BiSS license for applications and the stability and continuity of the protocol itself since its introduction.

BiSS Line follows the industrial trend of fully digital communication, functional safety capabilities and motor power supply over a single cable. However, BiSS Line provides all specific features of BiSS C. The data transmission is based on the industrial standard RS-485 and is protected by forward error correction (FEC) against disturbances coupled from the motor line to the data line. The possible cycle time for process data of e.g. 128 bit and for example a cable length up to 100 m is about 62.5 µs with FEC and 31.25 µs without FEC.

BiSS LINE STRUCTURE

The BiSS Line system includes a single master and a single or multiple slaves. The process data and the device supply are transmitted over a single cable. The standard BiSS Line Drive consists of the blocks BiSS Line master (BLM), oscillator and RS-485 bus transceiver. The standard BiSS Line Device consists of the blocks RS-485 bus transceiver, DC/DC converter, BiSS Line slave (BLS), oscillator and the BiSS-C slave(s).

Figure 1 shows the 2-wire configuration which requires passive elements for power supply coupling.

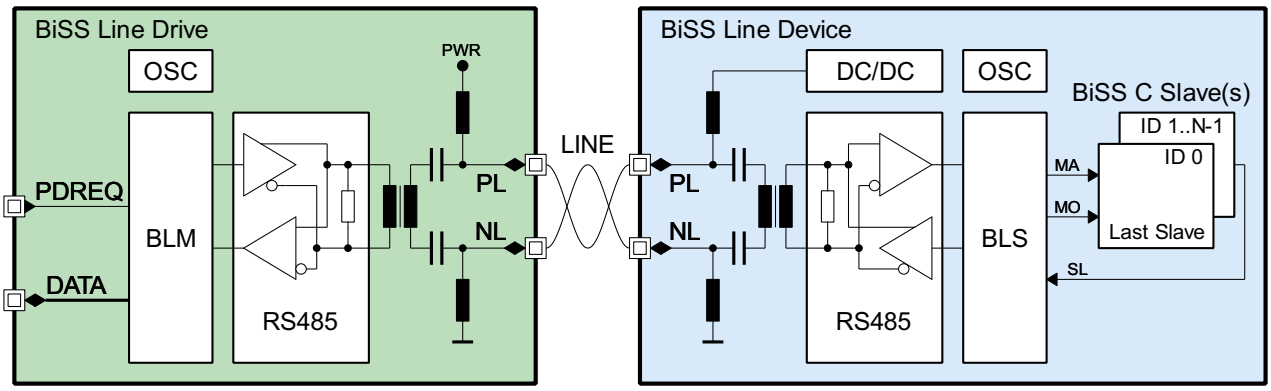

Figure 1: BiSS Line 2-wire configuration

The 4-wire connection with separate power lines is shown in Figure 2.

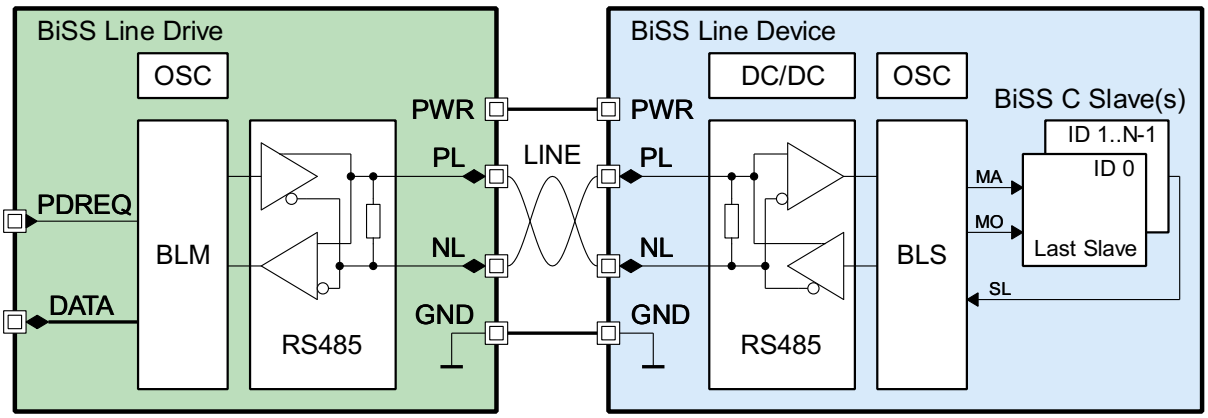

Figure 2: BiSS Line 4-wire configuration

BiSS LINE PROTOCOL

BiSS Line Frame

The BiSS Line communication is realized with frames using a RS-485 half-duplex baseband serial transmission. A frame is initiated by the master and usually finished by a slave. In between frames, the master sends an IDLE signal to prevent a DC charge of the line. At the beginning of a frame, the master interrupts the IDLE signal and sends one of several START signals followed by the DATA. When the master stops the transmission, the slave sends the response starting with the IDLE signal, followed by the START signal RSP and the DATA. Afterwards, the master sends the IDLE signal again until the next frame begins.

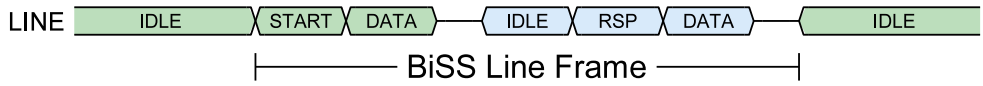

Figure 3: BiSS Line Frame

IDLE Signal

The IDLE signal is an alternating code with high frequency suitable for clock recovery. The length is not determined and the master can abort the IDLE signal after any zero bit. A long IDLE signal may help the receiver to learn the phase of the LINE signal in disturbed environments. Additionally, it is possible to detect the clock frequency.

START Signal

The codes of the START signals are carefully chosen to provide a good distinction between each other and the IDLE signal. Figure 4 shows the Hamming Distance between the received code, which is loaded into a 14 bit wide register, and a comparative value. During IDLE and transmission of a START signal, the hamming distance is always five and above. At the moment when the START signal is received completely, the hamming distance becomes zero. This allows the receiver to reconstruct the end of the START signal exactly even if one or two bits flipped during transmission.

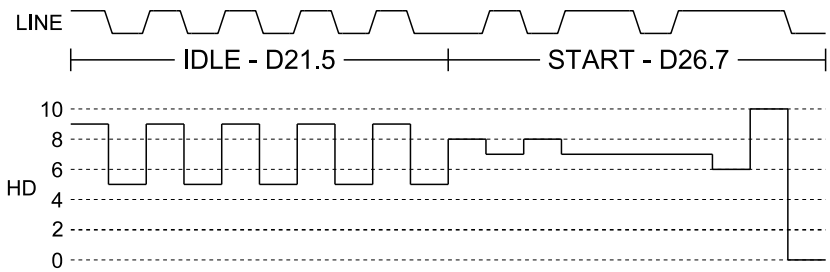

Figure 4: BiSS Line IDLE and START signal

Process Data Frame

The capturing of process data is usually triggered by the drive. Typically, it is not synchronized to the data on the LINE. BiSS Line is able to minimize the jitter between the position request from the drive and the latch event in the sensor. Therefore, the delay TDLY between the trigger event and a rising edge on LINE is measured and transmitted after REQ, which is used as START signal for the Process Data Frame (Figure 5). When the BiSS Line slave receives REQDLY, it adds a delay of TDLY before starting the BiSS C frame to ensure equidistant data acquisition. The REQDLY is also coded with a Hamming Distance to enable error correction.

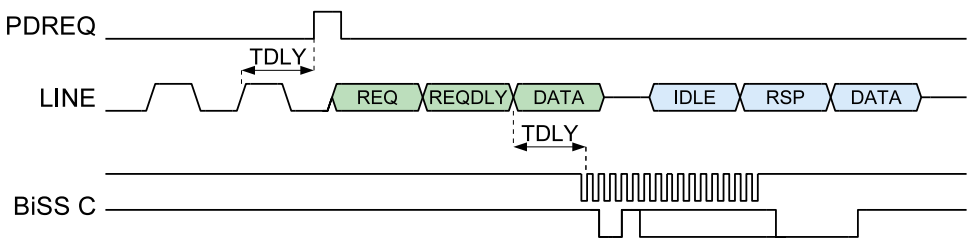

Figure 5: Process Data Frame

Process Data
The Process Data is divided into data channels. Usually, each data channel is transmitted completely in every Process Data Frame. But for low frequency data, e.g. temperature, the data channel can be configured to be transmitted segmentedly in several frames.
The Process Data is 8B10B coded with the benefit of DC balance and sufficient transitions for clock recovery. A forward error correction (FEC) for Process Data can be used optionally. To reduce the error rate in disturbed environments, the Process Data can be transmitted repeatedly by request or pre-configuration.
Additionally, a sector within the Process Data can be reserved to request further data.

Config Frame
The Config Frame is used at startup to configure the BiSS Line communication parameter such as the number of data channels and the data length etc. The START signal for configuration is CMD followed by an opcode. Furthermore, CMD can be used in generally, to trigger frames, which do not require new Process Data like repeated transfer of lost or damaged data.

DEFINITIONS

Abbr.	Description
IDLE	IDLE signal send between Frame to prevent a DC charge of the line
REQ	START signal for the Process Data Frame
RSP	START signal for the Slave response
CMD	START signal for frames without Process Data Request (e.g. Configuration Frames)
PDREQ	Process Data Request from drive
REQDLY	Transmitted delay information to minimize the jitter of Process Data Request
TDLY	Measured delay between drive-sided trigger event and LINE clock
BLM	BiSS Line Master
BLS	BiSS Line Slave
PL	Positive line (master and slave)
NL	Negative line (master and slave)
LINE	BiSS Line communication and optional supply cable
RS485	Standard defining electrical characteristics of drivers and receivers for serial communications systems, also known as TIA/EIA-485
DC/DC	DC-to-DC converter and regulator
OSC	Oscillator
DATA	Relevant data to be transmitted
8B10B	Line code that maps 8 bit symbols to 10 bit symbols, DC balanced, good clock recovery
D21.5	8B IDLE symbol
D26.7	8B START symbol for Process Data Frame
FEC	Forward Error Correction
HD	Hamming Distance

Table 1: Explanations