

### BiSS C REGISTER WRITE DETAILS

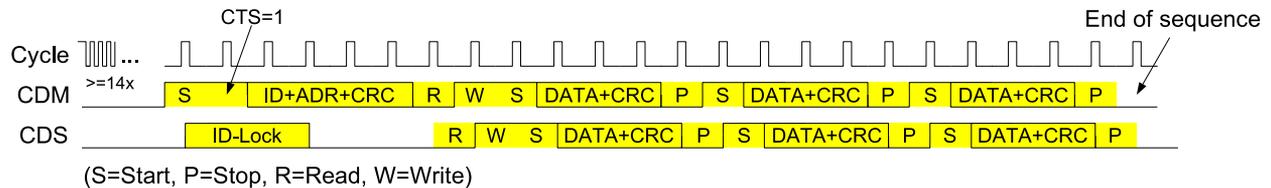


Figure 1: BiSS register write access

### TRAILING 0

The default state of the CDM bit is 0. To ensure that an previously started but aborted control communication frame is not continued a minimum set of 14 x 0 CDM bits are needed to be sent before a new control frame may be started.

The slaves do respond on this CDM default state with the CDS default state 0.

### S START BIT

The START bit is 1 and indicates the start of any control frame. There is no control frame started without a START bit. The START bit is not encapsulated by any CRC.

The IDL bits show the presence of IDs on the BiSS bus. Each present slave ID will be indicated as one IDL (ID LOCK). The IDL0 ... IDL7 are indicated. The ID locking is important for the slave and the master: the master can detect what ID range is occupied, the slaves occupy their individual IDs with this IDL sequence. All IDs from the smallest IDL0 to the highest present IDs are occupied. There will be no gap on IDs or IDLs. The IDL0 bit is first.

### CTS

For register access the CTS bit is always 1.

The slaves do still execute the IDL response while CTS.

### ID[2...0]

The ID does address the slave. Three ID bits are sent, MSB first.

The slave with three matching ID will respond and all other slaves not. The slaves do still execute the IDL response while ID[2...0].

### ADR[6...0]

The address does indicate the first register address of the ID selected slave. The address range of 7 bit ADR addresses 128 register bytes, MSB first.

The slaves do still execute the IDL response while ADR[6...0].

### CRC (AFTER ADR)

This CRC covers after the START bit, the CTS, ID and ADR address of the control frame. The used CRC polynome is  $X^4 + X^1 + X^0$  as is 0b10011. The start value for the CRC calculation is 0x00. The CRC result is transmitted inverted on the 4 CRC bit position. The CRC result generated by the master is verified by the slave. If the slave does detect a differing CRC result to the CRC result from the master, the access is refused and not executed by the slave.

The slaves do still execute the IDL response while CRC or do output the default CDS state 0.

### R READ BIT

On register write control frames the R bit is 0. The R bit is not encapsulated by any CRC. The inverted state of the R bit is transmitted by the W bit.

The slave does respond the received R bit.

### W WRITE BIT

On register write control frames the W bit is 1. The W bit is not encapsulated by any CRC. The inverted state of the W bit is transmitted by the R bit.

The slave does respond the received W bit.

### S START BIT

The START bit = 1 indicates the request of data. The START bit is not encapsulated by any CRC. There is no control frame started without a START bit. If the slave is not capable to respond directly, the START is repeated by the master until the slave is capable to respond.

The slave does respond the received START bit to the master. If the slave is not capable to respond directly, the START response is delayed by sending 0 bits. With being able to respond the requested control communication, the slave does respond a START bit = 1.

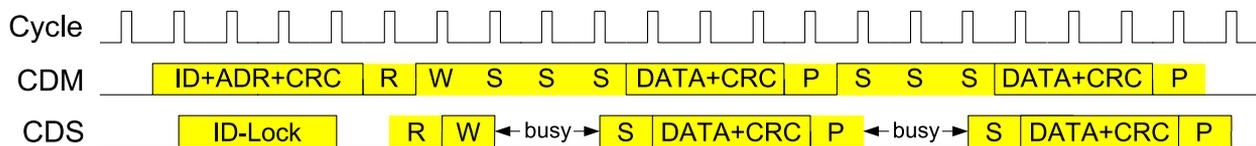


Figure 2: Delayed *BiSS* register write access

### DATA[7...0]

The DATA does carry the register content of the ID selected slave and the ADR addressed register. The DATA has 8 bit, MSB first.

The slave does respond the received DATA bits to the master.

### CRC (AFTER DATA)

This CRC covers after the START bit the DATA of the control frame only. The used CRC polynome is  $X^4 + X^1 + X^0$  as is 0b10011. The start value for the CRC calculation is 0x00. The CRC result is transmitted inverted on the 4 CRC bit position. The CRC result generated by the master is verified by the slave. If the slave does detect a differing CRC result to the CRC result from the master, the access is refused and not executed by the slave.

The slave does respond the received CRC bits to the master.

### P STOP BIT

On control frames the STOP bit is 0. The STOP bit is not encapsulated by any CRC.

The slave does respond the received STOP bit to the master.

### ADDITIONAL S START BIT

An additional START bit that is 1 indicates following optional DATA bytes that are addressed by the next followed address to the previously addressed DATA. The START bit is not encapsulated by any CRC.

The slave does respond the received START bit to the master.

### EXAMPLE 1 REGISTER WRITE

This example shows the PRESET function of iC-LGC. Writing the command register in address 0x60 with the command PRESET = 0x02 the internal PRESET sequence of iC-LGC is executed. The only BiSS slave device connected to the BiSS master is the iC-LGC. It does occupy only one slave ID. It's slave ID is 0b000.

The CRC result of the binary sequence 0b1 000 110.0000 ( CTS, ID[2:0], ADR[6:0] ) and the CRC polynome 0b10011 and the start value of 0x00 is 0b0100. The inverted CRC calculation result result is transmitted as CRC[3:0] = 0b1011.

The crc result of the binary sequence 0b0000.0010 ( DATA[7:0] )and the crc polynome 0b10011 and the start value of 0x00 is 0b0110. The inverted crc calculation result is transmitted as CRC[3:0] = 0b1001.

Cycle	1...14	15	16	17..19	20..26	27..30	31	32	33	34..41	42..45	46
Data	14 * 0	S	CTS	ID(2:0)	ADR(6:0)	CRC(3:0)	R	W	S	DATA(7:0)	CRC(3:0)	P
CDM	14 * 0	1	1	000	0b1100.000	0b1011	0	1	1	0000.0010	0b1001	0

Table 1: BiSS Control-Frame: write 0x60

### EXAMPLE 2 REGISTER WRITE

This example shows how to programm the resolution of iC-MH. Writing the command register in address 0x06 with the parameter SELRES[7:0] = 0x82 for the interpolation factor x1024 and a resolution of 8192. The only BiSS slave device connected to the BiSS master is the iC-MH. It does occupy only one slave ID. It's slave ID is 0b000.

The CRC result of the binary sequence 0b1 000 000.0110 ( CTS, ID[2:0], ADR[6:0] ) and the CRC polynome 0b10011 and the start value of 0x00 is 0b0011. The inverted CRC calculation result result is transmitted as CRC[3:0] = 0b1100.

The crc result of the binary sequence 0b1000.0010 ( DATA[7:0] )and the crc polynome 0b10011 and the start value of 0x00 is 0b1000. The inverted crc calculation result is transmitted as CRC[3:0] = 0b0111.

Cycle	1...14	15	16	17..19	20..26	27..30	31	32	33	34..41	42..45	46
Data	14 * 0	S	CTS	ID(2:0)	ADR(6:0)	CRC(3:0)	R	W	S	DATA(7:0)	CRC(3:0)	P
CDM	14 * 0	1	1	000	0b000.0110	0b1100	0	1	1	1000.0010	0b0111	0

Table 2: BiSS Control-Frame: write 0x06

### BiSS C REGISTER READ DETAILS

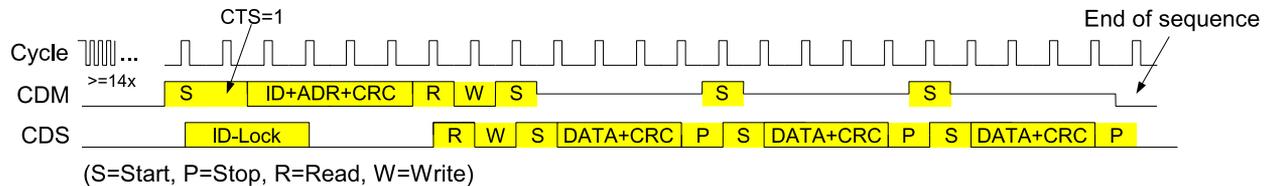


Figure 3: BiSS register write access

### TRAILING 0

The default state of the CDM bit is 0. To ensure that an previously started but aborted control communication frame is not continued, a minimum set of 14 x 0 CDM bits are needed to be sent before a new control frame may be started.

The slaves do respond on this CDM default state with the CDS default state 0.

### START BIT

On control frames the START bit is 1. The START bit is not encapsulated by any CRC. There is no control frame started without a START bit.

The IDL bits show the presence of IDs on the BiSS bus. Each present slave ID will be indicated as one IDL. The IDL0 ... IDL7 are indicated. The ID locking is important for the slave and the master: the master can detect what ID range is occupied, the slaves occupy their individual IDs with this sequence. All IDs from the smallest ID0 to the highest present IDs are occupied. There will be no gap on IDs or IDLs.

### CTS

For register access the CTS bit is always 1.

### ID[2...0]

The ID does address the slave. Three ID Bits are sent, MSB first.

The ID with three matching ID will respond and all other slaves not. The slaves do still execute the IDL response while ID[2...0].

### ADR[6...0]

The address does indicate the first register address of the ID selected slave. The address range of 7 bit ADR addresses 128 register bytes, MSB first.

The slaves do still execute the IDL response while ADR[6...0].

### CRC (AFTER ADR)

This CRC covers after the START bit the CTS, ID and address of the control frame. The used CRC polynome is  $X^4 + X^1 + X^0$  as is 0b10011. The start value for the CRC calculation is 0x00. The CRC result is transmitted inverted on the 4 CRC bit position. The CRC result generated by the master is verified by the slave. If the slave does detect a differing CRC result to the CRC result from the master, the access is refused and not executed by the slave.

The slaves do still execute the IDL response while CRC or do output the default CDS state 0.

### R READ BIT

On register read control frames the R bit is 1. The R bit is not encapsulated by any CRC. The inverted state of the R bit is transmitted by the W bit.

The slave does respond the received R bit to the master.

### W WRITE BIT

On register read control frames the W bit is 0. The W bit is not encapsulated by any CRC. The inverted state of the W bit is transmitted by the R bit.

The slave does respond the received W bit to the master.

### S START BIT

On control frames the START bit bit is 1. The START bit is not encapsulated by any CRC. There is no control frame started without a START bit. If the slave is not capable to respond directly, the START is repeated by the master until the slave is capable to respond.

The slave does respond the received START bit to the master with one frame delay. If the slave is not capable to respond directly, the START is delayed by sending 0 bits. With beeing able to respond the requested control communication, the slave does respond a START bit.

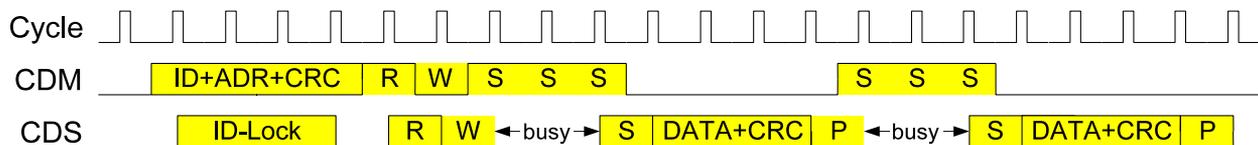


Figure 4: Delayed BiSS register read access

### PLACEHOLDER DATA 8 x 0

The master does send 8 bit 0 as placeholder for data.

The slave does respond the received DATA bits to the master.

### PLACEHOLDER CRC 4 x 0

The master does send 4 bit 0 as placeholder for CRC.

### P STOP BIT

On control frames the STOP bit is 0. The STOP bit is not encapsulated by any CRC.

The slave does respond the received STOP bit to the master.

### ADDITIONAL S START BIT

An additional START bit that is 1 indicates following optional DATA bytes that are addressed by the next followed address to the previously addressed DATA. The START bit is not encapsulated by any CRC.

# BiSS Interface

## AN11: BiSS C REGISTER ACCESS DETAILS



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### EXAMPLE 3 REGISTER READ

This example shows to read the status of iC-LGC.

Reading the register 0x60 of iC-LGC returns its status. The only BiSS slave device connected to the BiSS master is the iC-LGC. It does occupy only one slave ID. It's slave ID is 0b000.

The crc result of the binary sequence 0b1 000 110.0000 ( CTS, ID[2:0], ADR[6:0] ) and the crc polynome 0b10011 and the start value of 0x00 is 0b0100. The inverted crc calculation result result is transmitted as CRC[3:0] = 0b1011.

The placeholder for DATA[7:0] carries 0.  
The placeholder for CRC[3:0] carries 0.

Cycle	1...14	15	16	17..19	20..26	27..30	31	32	33	34..41	42..45	46
Data	14 * 0	START	CTS	ID(2:0)	ADR(6:0)	CRC(3:0)	R	W	START	DATA(7:0)	CRC(3:0)	Stop
CDM	14 * 0	1	1	000	0b1100.000	0b1011	1	0	1	0000.0000	0b0000	0

Table 3: BiSS Control-Frame: read 0x60

### EXAMPLE 4 REGISTER READ

This example shows how to read the status messages of iC-MH.

Reading the register in address 0x76 and 0x77 returns the GAIN and the status flags of iC-MH. The only BiSS slave device connected to the BiSS master is the iC-MH. It does occupy only one slave ID. It's slave ID is 0b000.

The crc result of the binary sequence 0b1 000 111.0110 ( CTS, ID[2:0], ADR[6:0] ) and the crc polynome 0b10011 and the start value of 0x00 is 0b1011. The inverted crc calculation result result is transmitted as CRC[3:0] = 0b0100.

The placeholder for DATA[7:0] carries 0.  
The placeholder for CRC[3:0] carries 0.

The second byte read is the following address (0x77) to the previously address (0x76).

Cycle	1...14	15	16	17..19	20..26	27..30	31	32	33	34..41	42..45	46	47	48..55	56..59	60
Data	14 * 0	S	CTS	ID(2:0)	ADR(6:0)	CRC(3:0)	R	W	S	DATA(7:0)	CRC(3:0)	P	S	DATA(7:0)	CRC(3:0)	P
CDM	14 * 0	1	1	000	0b111.0110	0b0100	1	0	1	0000.0000	0b0000	0	1	0000.0000	0b0000	0

Table 4: BiSS Control-Frame: read 0x76 + 0x77