BiSS Interface
AN18: BiSS C ANALYZER

CONTENTS

BASIC OPERATION

The BiSS AN18 explains how to analyze an external BiSS communication with a logic analyzer and the BiSS C protocol analyzer plug in. The BiSS C sensor data (point-to-point) single cycle data (SCD) and BiSS C register access are analyzable.

The basic operation of the BiSS logic analyzer is based on:

- Saleae USB logic analyzer hardware (logic or logic16)
- Saleae USB logic analyzer software
- iC-Haus logic analyzer software protocol extension (DLL) for BiSS C

Figure 1: device logic

Figure 2: device logic16

Clock rates

To analyze a BiSS communication with clock rates $\leq$ 2 MHz the logic analyzer is typically sufficient.
For dedicated BiSS clock rates please check the analyzer capabilities.

Attention: On PC-BiSS adapter and PC software based BiSS communication the MA clock rate may be configurable in the software e.g. to 2 MHz.

BiSS analyzer modes
Position data:

- Serial Data/Position 9 - 64 bit (selectable)
- NERR (low active error flag)
- NWARN (low active warning flag)
- CRC 6 bit (based on 0x43 CRC polynomial)

Register communication:

- read access
- sequential read access
- write access (only without delay time)

ANALYZER SOFTWARE

The compatible logic analyzer software is **Logic Software 1.1.15**.

See also:
→ http://www.saleae.com/
See also:
→ http://www.BiSS-Interface.COM/

BiSS ANALYZER INSTALLATION

The logic analyzer needs to be installed completely and all files and functions are needed to be accessible by the users standard logic analyzer operation.

ELECTRICAL INTERFACE

RS422 BiSS Encoder Interface
The typical electric interface of a BiSS communication is an RS422/RS485 link between BiSS master(drive) and BiSS slave(sensor).

Embedded BiSS Interface
On embedded applications TTL signals are directly accessible. The logic analyzer works with standard TTL thresholds. The logic16 analyzer works with two different threshold settings one for 1.8V to 3.6V and another one for 3.6V to 5V.

Electrical power supply and Ground connection
To run the analyzer, a GND Ground connection is mandatory and needs to be connected first.
To run the analyzer, a supply of optional interface adapters is mandatory.

Attention: Please ensure the correct connection sequence and input voltage ranges of all devices.

Attention: Please ensure the correct signal connection on positive signal of MA and SL.

Attention: Please ensure that there is no line delay compensation required for the logic analyzer.
This is uncritical on short cable lengths and standard MA clock frequencies or the capturing with the logic analyzer close to the BiSS sensor and not close to the BiSS master.

ANALYZER SOFTWARE CONFIGURATION

Adding the BiSS protocol

After the start of the Logic software You can add the BiSS C protocol to the analyzer (”+” pull down).

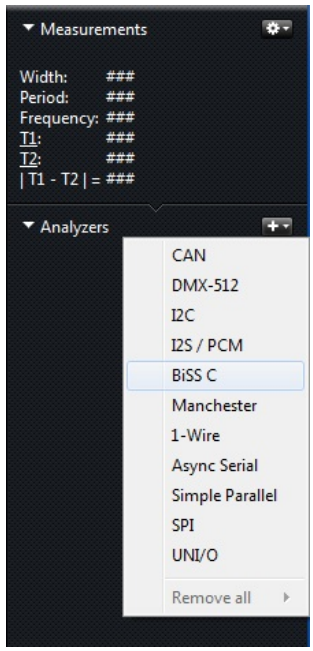

Figure 3: Add analyzer

Analyzer Settings for single cycle data communication

The ”analyzer settings” window opens and needs the following setting:

- Which logic analyzer channels capture the signals
  - MA: master clock output (= MA output of the master)
  - SLO: slaves data output (= SL input of the master)
- What type of data / communication to be analyzed
  - Single Cycle Data communication of BiSS C or BiSS C unidirectional
- Serial data length (only the length of sensor data excluding two standard flags and the standard 6 bit CRC))

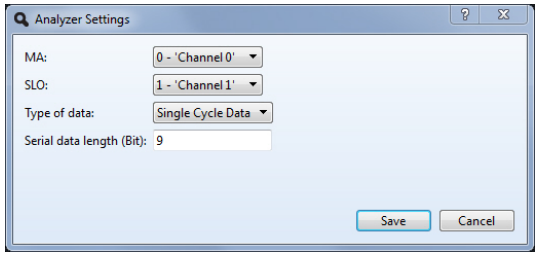

Figure 4: Configure the Analyzer settings

Analyzer Settings for register data communication
The ”analyzer settings” window opens and needs the following setting:

- Which logic analyzer channels capture the signals
  - MA: master clock output (= MA output of the master)
  - SLO: slaves data output (= SL input of the master)
- What type of data / communication to be analyzed
  - Register Data communication

Note: The serial data length setting is not necessary for the register data communication.

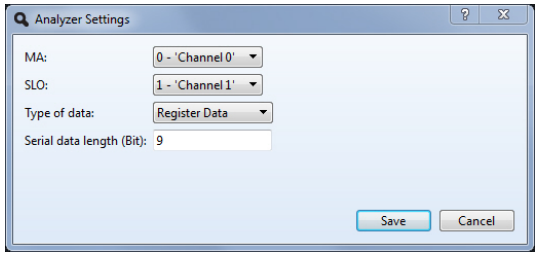

Figure 5: Configure the Analyzer settings

Renaming the channels
Rename the two used channels to the BiSS signal names:

- MA: master clock output (= MA output of the master)
- SLO: slaves data output (= SL input of the master)

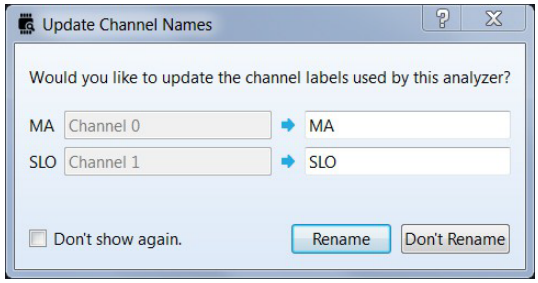

Figure 6: Rename Analyzer signals

Configure trigger and capturing
The analyzer requires the BiSS conform capturing and trigger configuration:

- Number of samples to be captured
- Capturing frequency
- Channel to trigger on (only one channel possible)
- Falling edge to trigger on

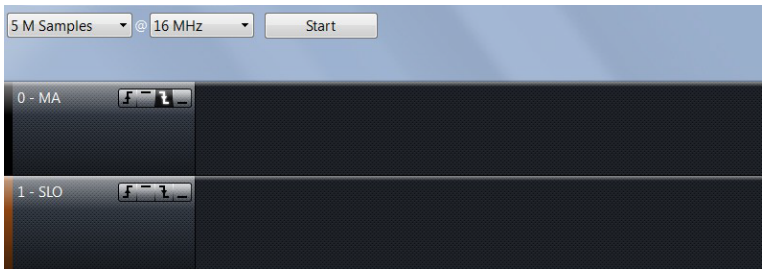

Figure 7: Configure channel, edge, samples, frequency

- Confirm configuration with ”Start” button

Capturing active
The capturing is now active and waits on trigger events to capture. The analysis is now available.

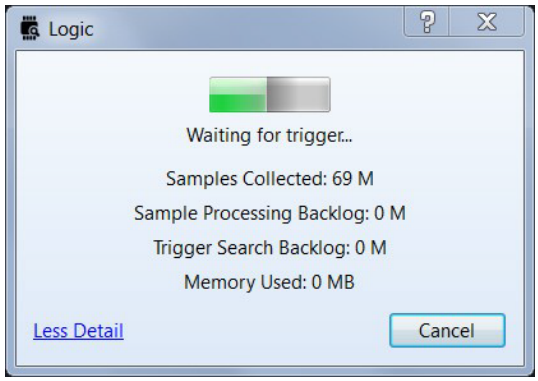

Figure 8: Active capturing

BiSS SINGLE CYCLE DATA FRAME

Complete SCD frame

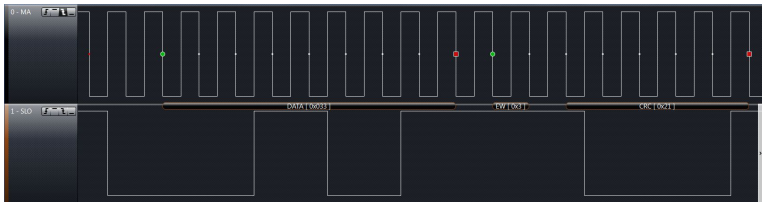

Figure 9: *BiSS* Single Cycle Data frame

The protocol analyzer DLL expects the length of sensor data excluding two standard flags and the standard 6 bit CRC. The 2 flags and the inverted 6 bit CRC are considered automatically. Here a BiSS C sensor with a 24 position data + 2 flags + 6 bit CRC that is transmitted inverted configuration will look like this:

Figure 10: Example SCD: 24 bit sensor data + 2 flags + 6 bit CRC

A corresponding BiSS reader configuration of a 24 position data + 2 flags + 6 bit CRC that is transmitted inverted will look like this:

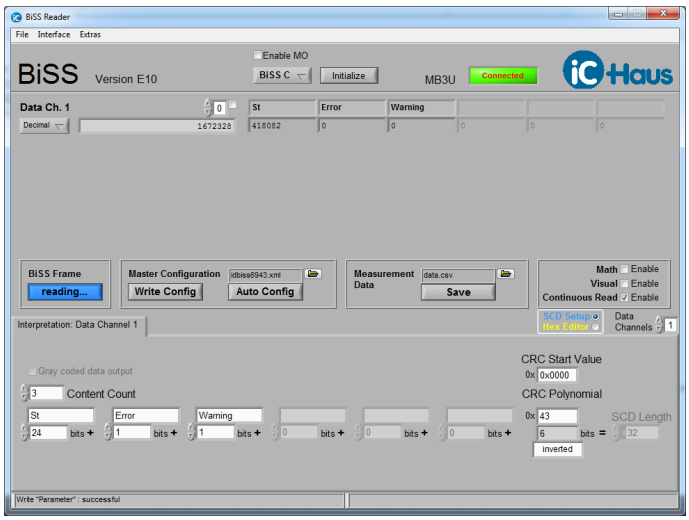

Figure 11: Related BiSS Reader configuration on the example SCD: 24 bit sensor data + 2 flags + 6 bit CRC

Attention: The CRC results are only captured values.
There is no automated verification of CRC results in the BiSS analyzer plug in.

BiSS REGISTER ACCESS

Complete Register access

Figure 12: *BiSS* control communication for register access

Note: Please ensure that the selected sample depth is sufficient to show a complete register access.

Attention: The CRC results are only captured values.
There is no automated verification of CRC results in the BiSS analyzer plug in.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2010-06-09		Initial release	

Rel.	Rel. Date*	Chapter	Modification	Page
A2	2013-01-25	BASIC OPERATION	Minor updates regarding long SCD data lengths up to 64 bit	1

Rel.	Rel. Date*	Chapter	Modification	Page
A3	2015-11-11	BASIC OPERATION	For dedicated BiSS clock rates please check the analyzer capabilities.	1
		ANALYZER SOFTWARE CONFIGURATION	Single Cycle Data communication: BiSS C or BiSS C unidirectional	3
		ANALYZER SOFTWARE CONFIGURATION	Added at Serial data length: (only the length of sensor data excluding two standard flags and the standard 6 bit CRC)	3
		ANALYZER SOFTWARE CONFIGURATION	Adding details: MA: master clock output (= MA output of the master) SLO: slaves data output (= SL input of the master)	3 + 4
		BiSS SINGLE CYCLE DATA FRAME	SCD example added: 24 bit sensor data + 2 flags + 6 bit CRC	6

* Release Date format: *YYYY-MM-DD*