PREAMBLE

For absolute position encoder, the serial BiSS interface is now used standard for fast and secure transmission of absolute measurement data. Thanks to the line delay compensation in the master high clock frequencies are possible, thanks to a CRC protected transmission bit errors are detected.

BiSS timeout: a feature of the BiSS sensor

The BiSS timeout is a feature of the BiSS sensor and its implementation. The BiSS timeout is generated by the sensors internal oscillator. When using BiSS, the BiSS timeout of the sensor may vary. For master defined high clock frequencies short timeouts are possible. For master defined low clock frequencies long timeouts are mandatory. Many BiSS sensors permit a RAM or ROM based configuration for a short or long BiSS timeout.

BiSS sensors with an adaptive BiSS timeout do not need to be configured for a short or long BiSS timeout. BiSS sensors adapts the own BiSS timeout to the master clock frequency. Therefor the BiSS sensor with adaptive BiSS timeout measures the master clock frequency and generates an adapted (short or long) BiSS timeout.

This BiSS Application Note describes details, effects and application solutions for the adaptive BiSS timeout.

Figure 1: BiSS Frame with timeout
The BiSS timeout may be a constant timeout or an TMA-adaptive BiSS timeout.

![BiSS frame with constant BiSS timeout](image)

**Figure 2: BiSS frame with constant BiSS timeout**

The benefit of the adaptive BiSS timeout is that even on a wide variety of MA clock frequency ranges the BiSS slave does not need a timeout reconfiguration. A BiSS slave will provide a long BiSS timeout on low MA clock frequencies and a short BiSS timeout on high MA clock frequencies. The adaptive BiSS timeout is learned by the BiSS slave on the first 1.5 periods of the MA clock. The adaptive BiSS timeout is updated by the BiSS slave with every new BiSS SCD cycle.

**BiSS adaptive timeout with single MA period**

In case of a single MA period (single falling and single rising edge on the MA line) the measurement for 1.5 TMA is no possible and the BiSS slave will use the default = maximum timeout length.

The maximum timeout length of the BiSS slave is expected to be 20 μs.

![Single MA period and default adaptive timeout](image)

**Figure 3: Single MA period and default adaptive timeout**

As the SL line is persisting high the master can not detect the BiSS slaves operated BiSS timeout of approximately 20 μs.

The BiSS master needs to ensure that the BiSS SCD cycle rate exceeds the default = maximum timeout length of the BiSS slave of approximately 20 μs.
DETAILS ON ADAPTIVE BiSS TIMEOUT JITTER

The BiSS communication faces two independent clock domains:

- MA clock of the BiSS master
- Sensor internal $f_{osc}$ oscillator frequency

![Figure 4: Rising edge jitter due to two clock domains](image)

The adaptive BiSS timeout length is learned by the BiSS slave. The count of slave $f_{osc}$ periods is learned for the first 1.5 TMA. After the BiSS SCD cycle the slave needs to output the learned timeout length. Due to two independent clock domains the variation may be a whole TMA and a whole TOSC.

![Figure 5: Rising edge jitter details due to two clock domains](image)
ADAPTIVE BISS TIMEOUT JITTER EXAMPLES

The iC-MHM uses an $f_{osc}$ of typically 14 MHz, the possible range is 11.5 ... 16 MHz over full supply range and temperature range. The MB5U uses an $f_{osc}$ of typically 20 MHz, the possible variance and tolerance is each 50 ppm over full supply range and temperature range.

Figure 6: 10 MHz MA clock and 500 nsec BiSS timeout
Figure 6 shows a adaptive BISS timeout of 4/5 DIV of 400 nsec/DIV = 500 nsec adaptive BISS timeout length. Minimum adaptive BISS timeout length is 1.5 x 100 nsec = 150 nsec.

Figure 7: 1 MHz MA clock and 1.5µsec BiSS timeout
Figure 7 shows a adaptive BISS timeout of 3/5 DIV of 4 µsec/DIV = 2.4 µsec adaptive BISS timeout length. Minimum adaptive BISS timeout length is 1.5 x 1 µsec = 1.5 µsec.
Figure 8 shows a adaptive BiSS timeout of 2/5 DIV of 40 µsec/DIV = 16 µsec adaptive BiSS timeout length. Minimum adaptive BiSS timeout length is 1.5 x 10 µsec = 15 µsec.

By a rule of thumb:
- the longer TMA of the master the shorter = better = closer to the possible minimum is the adaptive BiSS timeout
- the higher the fosc of the sensor the shorter = better = closer to the possible minimum is the adaptive BiSS timeout

### BiSS Slave Products Without Adaptive BiSS Timeout

The listed products do not provide an adaptive BiSS timeout (optional or exclusive):
- iC-LGC
- iC-MD
- iC-MH
- iC-MH8
- iC-MHL200
- iC-MN


### BiSS Slave Products With Adaptive BiSS Timeout

The listed products do provide the adaptive BiSS timeout (optional or exclusive):
- iC-MR (optional by NEADAP)
- iC-MHM
- iC-MH16 (optional by ENADAP)
- iC-MU
- iC-MU150 (optional by NTOA)
- iC-NQC (optional by TOA)
- iC-MCB (optional by NTOA = 0)
- MC1xx (optional by NEADAP)

Emulated BiSS master solutions may cause communication failures with BiSS slaves that provide the adaptive BiSS timeout. Such emulated BiSS master solutions might not be able to provide a constant MA period with no variation on pulse and pause timing. On a combination of BiSS slaves that provide the adaptive BiSS timeout and emulated BiSS master the BiSS communication may fail due to BiSS timeout within the SCD sequence. A solution to prevent a failing BiSS communication is the extended output of the leading periods of the MA clock. A BiSS slave with adaptive BiSS timeout uses the first 1.5 periods to learn the BiSS timeout. Expanding the duration of those 1.5 first MA periods solves the problem with the BiSS adaptive timeout.

![Figure 9: SCD frame with expanded first MA pause and adaptive BiSS timeout](image)

Typically an SPI interface is used to emulate the BiSS master. Any solution that expands the duration of the first 1.5 periods solves the situation. The most simple solution is expanding the first MA pause:

- Default MA clock state is MA = 1
- Set MA to 0
- Delay $t_{\text{pause}}$
- Set MA to 1
- Start the 1. clock set (WORD wide) on MA output
- Start the 2. clock set (WORD wide) on MA output
- Start the 3. clock set (WORD wide) on MA output
- ...

The given delay of $t_{\text{pause}}$ needs to be bigger than the expected clock delay from word-to-word clock set. In the case of an SPI based BiSS master emulation the delay from word-to-word clock set is often caused by unloading the received SPI content.

![Figure 10: SCD frame with expanded first MA pause emulated by SPI and adaptive BiSS timeout](image)

**BiSS BUS STRUCTURES WITH MIXED TIMEOUTS**

On BiSS bus structures the remaining BiSS timeout depends on the longest BiSS timeout in the BiSS bus daisy chain.
iC-Haus BiSS MASTER DEVICES, IPs, ADAPTERS

iC-Haus standard BiSS master ICs
All standard BiSS master ICs iC-MB3 TSSOP24, iC-MB4 TSSOP24 and iC-MB4 QFN28 provide a constant MA period with no variation on pulse and pause timing.

iC-Haus standard PC USB BiSS adapter
All standard BiSS adapter are iC and IP based. MB3U, MB3U-I2C, MB4U and MB5U provide a constant MA period with no variation on pulse and pause timing.

iC-Haus standard BiSS master IPs (VDHL)
All standard VHDL BiSS master IPs MB101, MB105, MB107, MB109 provide a constant MA period with no variation on pulse and pause timing.

iC-Haus software based BiSS master IP
The BiSS master device IP MB302 is GPIO port and also SPI based and may generate a variation on pulse and pause timing of the MA clock signal. Please documentation check for details.

REVISION HISTORY

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