BiSS C REGISTER ACCESS DETAILS

Structure of a single, complete SCD cycle

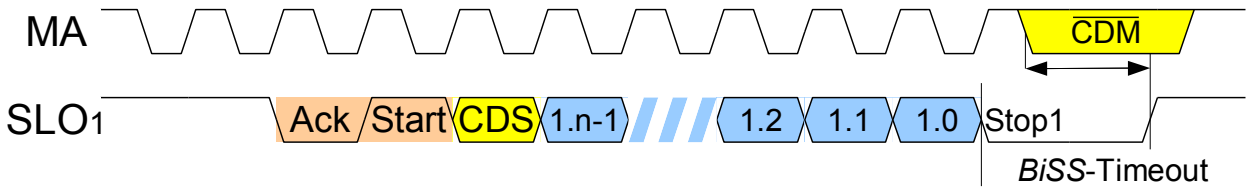

Figure 1: *BiSS* Frame (SCD point-to-point configuration)

- The CDM bit is transmitted inverted with the MA clock.
- The CDS bit is the response of a slave and this response is transmitted to the master in the following cycle.
- Every SCD cycle ends with a *BiSS* timeout.

Structure of a starting single register access

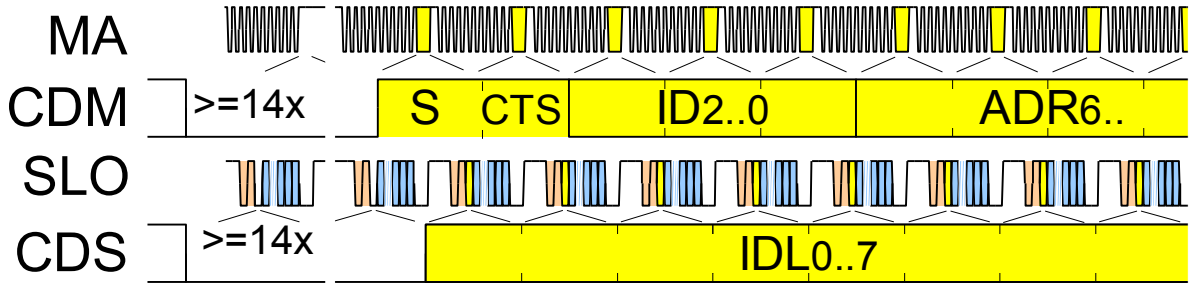

Figure 2: *BiSS* Frame (register access)

- Minimum 14 SCD cycles with ”CDM = 0” are required to abort a possible previouly started command frame.
- ”START = 1” indicates all slaves the start of a control communication.
- ”CTS = 1” indicates all slaves a register access.
- CDS indicates with the ”IDL” bits the master how many of the possible 8 *BiSS* IDs have been occupied.
- The "ID locking" informs every slave about its slave ID on the *BiSS* bus.