BiSS Interface
AN6: BiSS C DATA LENGTH DETECTION

BiSS C PROTOCOL DETAILS

With not knowing the present bit length of a BiSS C sensor a detection of the sensors data channel bit length and the polynome is possible.

The following analysis focuses on:

- Single slave system
- Single data channel
- Point to Point BiSS device

BiSS bus structures are also applicable with regards to a scaled behaviour.

APPLIED BiSS C POLYNOMES

The typical applied BiSS C polynomes are:

- 0x25 for bit length of up to 26 bit
- 0x43 for bit length of up to 57 bit

Typical BiSS C device CRC polynomes:

- iC-MH: always 0x43 CRC polynome, no start value option
- iC-MN: always 0x43 CRC polynome, start value optional
- iC-LGC: always 0x43 CRC polynome, start value optional
- iC-NQC: typical 0x43 CRC polynome, optional 0x25, no start value option
- MC103: always 0x43 CRC polynome, no start value option

BiSS Profile compliance
The Standard BiSS Profiles BP1 and BP3 support only the CRC polynome 0x43.

The following analysis focuses on:

- Single slave system
- Single data channel
- Point to Point BiSS device
- CRC start value 0b00 0000
- Standard BiSS CRC polynome 0x43

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NUMERIC DEPENDENCIES

CRC polynome length and CRC length

The CRC length is 1 bit smaller than the CRC polynome length. The CRC Polynome 0x43 = "0b100 0011" has a length of 7 bit. A CRC polynome with the length of 7 bit generates a 6 bit long CRC. The MSB of a reasonable CRC polynome is typically a "1".

The data "0b0000 0000 0000 11" and CRC Polynome = "0b100 0011" generates the CRC "0b00 0101".

Leading "0" do not change the CRC

Leading MSB bits that are "0" do not change the CRC result when the CRC startvalue is "0".

SCD data position

The SCD data position is left aligned. The MSB of the SCD is always identical to the MSB of the received data, independant to correct or wrong SCD data length configurations.

Clocking less SCD bits that present

The BiSS C protocol permits less clocking bits that present SCD bits, the data stream is stopped with the count of clocks. The clocking count needs to include the slaves CDS bit at minimum. A reasonable clocking count starts with 14 bit (12 position bit and 2 bit flags).
Clocking less SCD bits that present: the CRC is incomplete and possible to be invalid.

Clocking too many SCD bits that present

The BiSS C protocol permits BiSS bus structures. With clocking more SCD bits that present SCD bits, the data stream is extended by "0" bits after the slaves data. The clocking count needs to be limited to the maximum bit count of 57 bit sensors data (position and flags) and with a 6 bit CRC.
Clocking too many SCD bits that present: the CRC is delocated, extended by "0" bits and possible to be invalid.
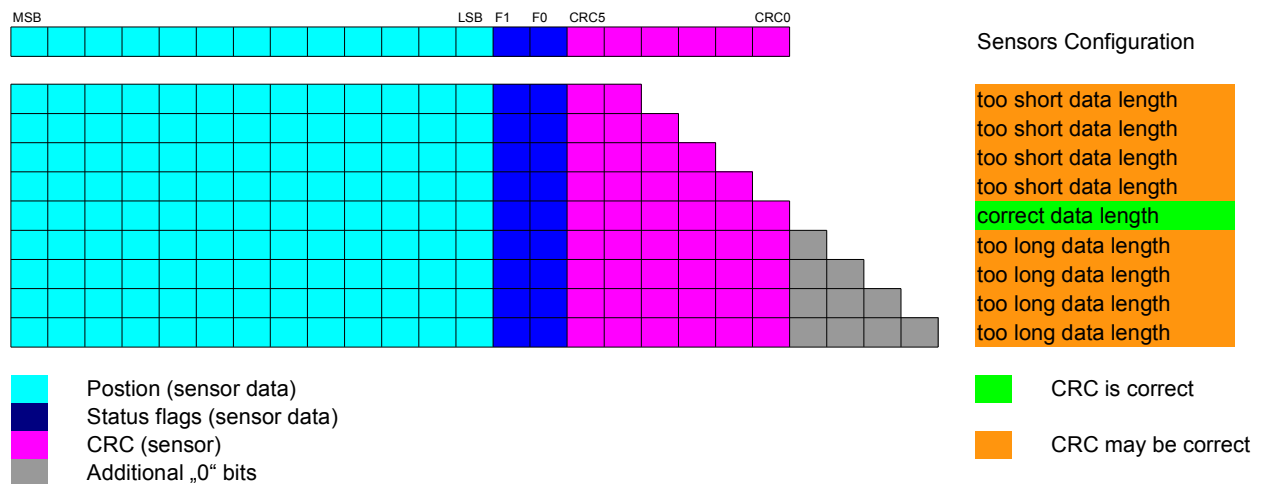

Figure 1: CRC delocation, lost bits, added "0" bits,

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ALGORITHMIC VERIFICATION

With the probability of having a 6 bit matching CRC code on an "n" bit long data stream: it is possible that there are multiple matchings on the CRC verification going through all bit lengths.

Reduce the range of data lengths to verify
The minimum BiSS C profile conform resolution is a 12 bit long postion plus 2 bit flags as are 14 bit minimum bit length. The maximum BiSS C profile conform resolution is a 55 bit long postion plus 2 bit flags as are 57 bit maximum bit length.

Assuming that the encoder position does not vary while verifying all bit lengths in the expected range, there might be a set of bit lengths that provide a correct CRC result.

By iteration those positions are needed to be verified by another encoder position than the previous used position generated a correct CRC result. With this loop: the reduction of positive CRC lengths will reduce to the real data length iteratively.
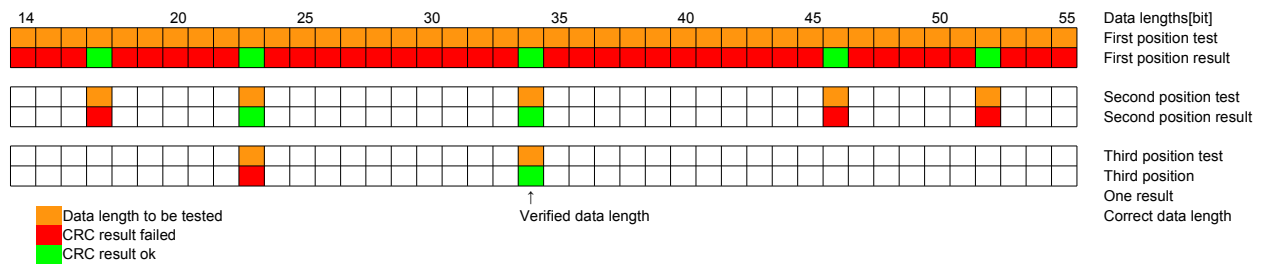

Figure 2: Iterative Data Length Scanning By Elimination

The smaller the range of possible bit length is

- the smaller is the count of data length verifications
- the smaller is the probability of matching CRC codes
- the smaller is the set of required encoder position interations

Observing 0b11 of flags
Assuming that the encoder position is valid and no error bit and no warning bit is preset (low as low active logic of both flags), the two following high bits in the data stream may indicate the flag position and reduce the count of iteration significant.