BiSS-Interface

BiSS EDS (COMMON PART)

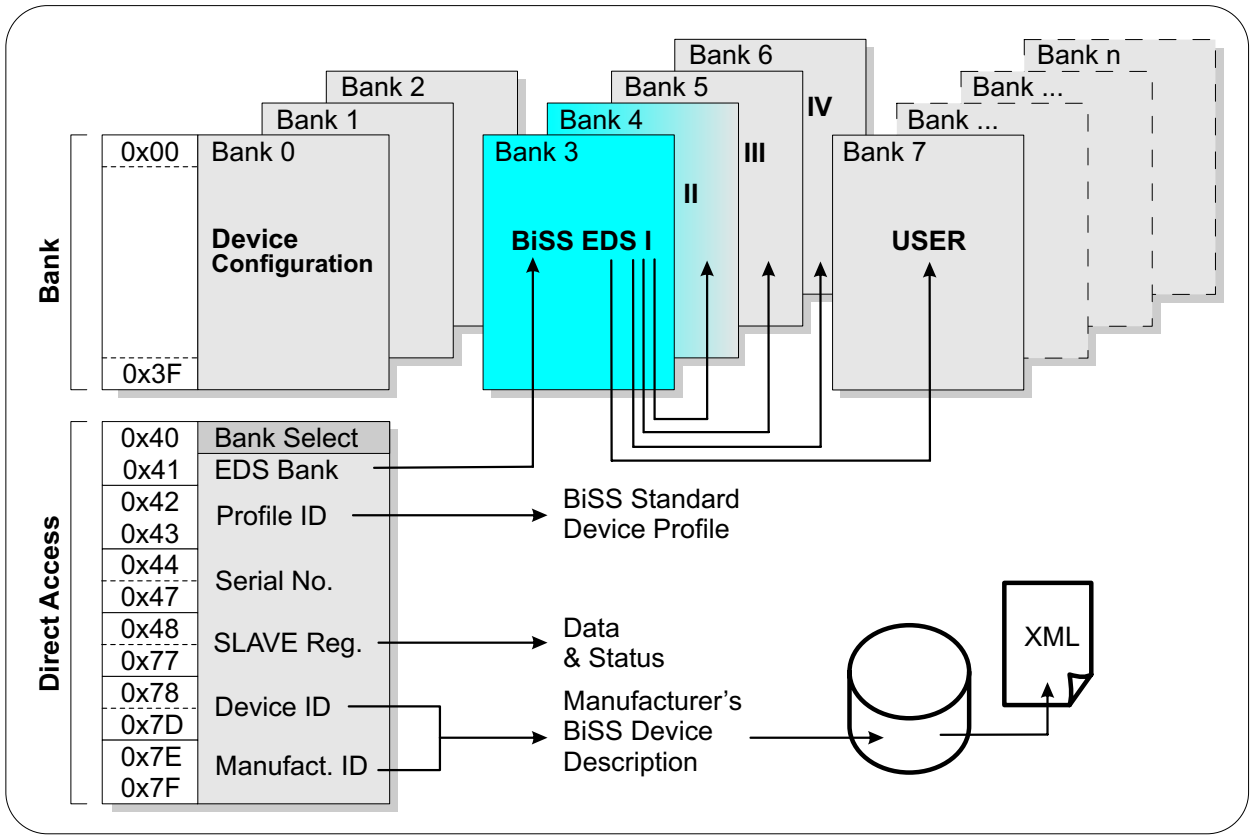
preliminary

FEATURES

- Common part of the *BiSS* EDS
- Standardised data format
- Simple control configuration

APPLICATIONS

- Fast and simple motion controller configuration
- Intelligent absolute rotary encoder



DESCRIPTION

The *BiSS* EDS (electronic datasheet) describes the attributes and operational conditions of a *BiSS* device and carries information about process data and parameter. The *BiSS* EDS is once per device available and describes all *BiSS* slaves inside this *BiSS* device.

The EDS starts on the bank that is defined in address 0x41 and may consist of multiple parts, where each part consists on one or multiple fully used banks.

The first part contains non process relevant information but the required information about data transmission and parameters for the master but no process data.

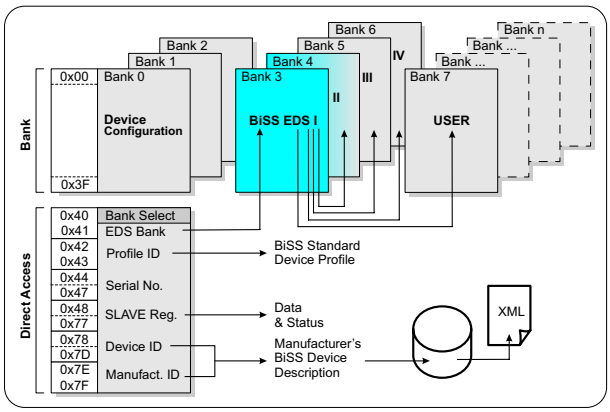


Figure 1: First, common part of the EDS

Hereto belongs clock frequency, timeout, delay timings etc. Additionally for every available data channel format, length and the starting bank address for profile depending content (second part of the EDS) is present.

This specification describes the common part of the *BiSS* EDS.

The second part contains required information about data transmission, product and process relevant information for the motion control system.

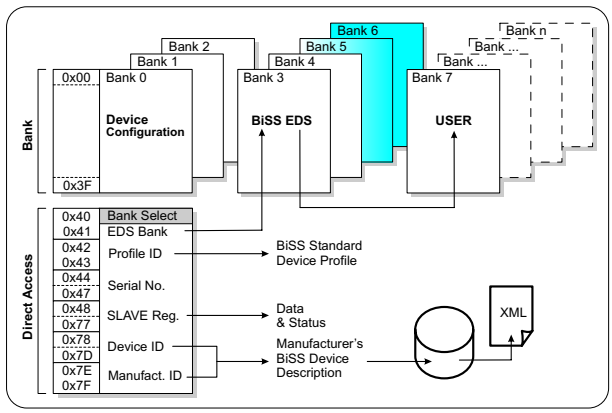


Figure 2: Second, profile specific part of the EDS

Hereto belong mechanical data, accuracy, structure of position values and product attributes.

The specification of the second EDS part, the *BiSS* profile specific EDS part, is located in the available *BiSS* profile documents.

ELECTRONIC DATA SHEET (COMMON PART)

Adr.	Symbol	Description	Group	Format	Unit	Values
0x00	EDS_VER	EDS version (continuous number)	Orga	U8	-	1 . . . 254
0x01	EDS_LEN	EDS length (bank count completely)	Orga	U8	Banks	1 . . . 254
0x02	USR_STA	Bank address USER start (bank selection in address 64, 255= not available)	Orga	U8	-	1 . . . 255
0x03	USR_END	Bank address USER end (bank selection address 64)	Orga	U8	-	1 . . . 254
0x04	TMA	Minimum permitted clock period on MA (TMA)	Timing	U8	1 ns	1 . . . 100
0x05	TO_MIN	Minimum *BiSS* timeout (0= adaptive)	Timing	U8	250 ns	0; 50 . . . 160
0x06	TO_MAX	Maximum *BiSS* timeout (0= adaptive)	Timing	U8	250 ns	0; 50 . . . 160
0x07	TOS_MIN	Minimum *BiSS* timeout_S (0= adaptive)	Timing	U8	25 ns	0; 20 . . . 120
0x08	TOS_MAX	Maximum *BiSS* timeout_S (0= adaptive)	Timing	U8	25 ns	0; 20 . . . 120
0x09	TCLK_MIN	Minimum sampling periode adaptive timeout (0= adaptives timeout not available)	Timing	U8	25 ns	0 . . . 254
0x0A	TCLK_MAX	Maximum sampling periode adaptive timeout (0= adaptives timeout not available)	Timing	U8	25 ns	0 . . . 254
0x0B	TCYC	Minimum cycle time (0= no limitation)	Timing	U8	250 ns	0 . . . 250
0x0C	TBUSY_S	Maximum processing time SCD	Timing	U8	250 ns	0 . . . 254
0x0D	BUSY_S	Additional processing time SCD in clocks	Timing	U8	TMA	0 . . . 254
0x0E 0x0F	PON_DLY	Maximum "power on delay" until control communication is available	Timing	U16 [1]	1 ms	0. . . 5000
0x10	DC_NUM	Number of data channel in this device (number of words)	SCD	U8	-	0 . . . 8
0x11	SL_NUM	Area of validity for this EDS (number of slave addresses)	SCD	U8	-	1 . . . 8
0x12	SL_OFF	Memory location for this EDS (slave ID within this device)	SCD	U8	-	0 . . . 7
0x13		Reserved				0
0x14	BANK1	Bank address for content description data channel 1 (profile EDS)	SCD	U8	-	0 . . . 254
0x15	DLEN1	Data length data channel 1	SCD	U8	bit	0 . . . 64
0x16	FORMAT1	Data format data channel 1	SCD	U8	bit	0 . . . 254
0x17	CPOLY1	CRC polynome(8:1) for data channel 1	SCD	U8	-	0 . . . 254
0x18	BANK2	Bank address for content description data channel 2 (profile EDS)	SCD	U8	-	0 . . . 254
0x19	DLEN2	Data length data channel 2	SCD	U8	bit	0 . . . 64
0x1A	FORMAT2	Data format data channel 2	SCD	U8	bit	0 . . . 254
0x1B	CPOLY2	CRC polynome(8:1) for data channel 2	SCD	U8	-	0 . . . 254
0x1C	BANK3	Bank address for content description data channel 3 (profile EDS)	SCD	U8	-	0 . . . 254
0x1D	DLEN3	Data length data channel 3	SCD	U8	bit	0 . . . 64
0x1E	FORMAT3	Data format data channel 3	SCD	U8	bit	0 . . . 254
0x1F	CPOLY3	CRC polynome(8:1) for data channel 3	SCD	U8	-	0 . . . 254
0x20	BANK4	Bank address for content description data channel 4 (profile EDS)	SCD	U8	-	0 . . . 254
0x21	DLEN4	Data length data channel 4	SCD	U8	bit	0 . . . 64
0x22	FORMAT4	Data format data channel 4	SCD	U8	bit	0 . . . 254

0x23	CPOLY4	CRC polynome(8:1) for data channel 4	SCD	U8	-	0 . . . 254
0x24	BANK5	Bank address for content description data channel 5 (profile EDS)	SCD	U8	-	0 . . . 254
0x25	DLEN5	Data length data channel 5	SCD	U8	bit	0 . . . 64
0x26	FORMAT5	Data format data channel 5	SCD	U8	bit	0 . . . 254
0x27	CPOLY5	CRC polynome(8:1) for data channel 5	SCD	U8	-	0 . . . 254
0x28	BANK6	Bank address for content description data channel 6 (profile EDS)	SCD	U8	-	0 . . . 254
0x29	DLEN6	Data length data channel 6	SCD	U8	bit	0 . . . 64
0x2A	FORMAT6	Data format data channel 6	SCD	U8	bit	0 . . . 254
0x2B	CPOLY6	CRC polynome(8:1) for data channel 6	SCD	U8	-	0 . . . 254
0x2C	BANK7	Bank address for content description data channel 7 (profile EDS)	SCD	U8	-	0 . . . 254
0x2D	DLEN7	Data length data channel 7	SCD	U8	bit	0 . . . 64
0x2E	FORMAT7	Data format data channel 7	SCD	U8	bit	0 . . . 254
0x2F	CPOLY7	CRC polynome(8:1) for data channel 7	SCD	U8	-	0 . . . 254
0x30	BANK8	Bank address for content description data channel 8 (profile EDS)	SCD	U8	-	0 . . . 254
0x31	DLEN8	Data length data channel 8	SCD	U8	bit	0 . . . 64
0x32	FORMAT8	Data format data channel 8	SCD	U8	bit	0 . . . 254
0x33	CPOLY8	CRC polynome(8:1) for data channel 8	SCD	U8	-	0 . . . 254
0x34	BC_OFF	Bus coupler control location for this device (slave ID within this device)	SCD	U8	-	0; 16 . . . 23
0x35		Reserved	Prot	U8	-	0
0x36		Reserved	Prot	U8	-	0
0x37		Reserved	Prot	U8	-	0
0x38		Reserved	Prot	U8	-	0
0x39		Reserved	Prot	U8	-	0
0x3A		Reserved	Prot	U8	-	0
0x3B		Reserved	Prot	U8	-	0
0x3C		Reserved	Prot	U8	-	0
0x3D		Reserved	Prot	U8	-	0
0x3E		Reserved	Prot	U8	-	0
0x3F	CHKSUM	Check sum (addition of all bytes within this bank)	Orga	U8	-	xx

Table 2: Electronic Data Sheet (common part)

[1)] The U16 value is saved as a Big Endian, i.e. with the highest-value byte at the lowest-value address.

DC_NUM	Addr. 0x10; bit 7:0	R
0x10	A *BiSS* device may use up to 8 data channel. This parameter indicates how many data channels on the *BiSS* bus are assigned to this device. Also data channels with a data length of ”0” are counted and assigned.	

Table 3: Count of data channels

SL_NUM	Addr. 0x11; bit 7:0	R
0x11	A *BiSS* device may occupy up to 8 slave IDs. This parameter indicates, how many slave IDs on the *BiSS* bus are assigned to this device. Even data channels data with a length of ”0” bit may occupy a slave IDs.	

Table 4: Area of validity for this EDS (count of slave addresses)

SL_OFF	Addr. 0x12; bit 7:0	R
0x12	A *BiSS* device may occupy up to 8 slave IDs. The storage location of the EDS (common part) is on one of these slave IDs. This parameter indicates, how many slave IDs are assigned before this slave ID on the *BiSS* bus within this device. This is appliable on combination of ”EDS storage capable” *BiSS* components and ”non EDS storage capable” *BiSS* components in one device.	

Table 5: Memory location for this EDS (slave ID offset within this device)

CHKSUM	Addr. 0x3F; bit 7:0	R
0x3F	The sum of all registers of the bank addresses 0x00 . . . 0x3E is stored as an 8 bit checksum in this register.	

Table 6: Checksum addition of all bytes of this bank

BC_OFF	Addr. 0x34; bit 7:0	R
0x00	No bus coupler present or controlable	
0x10	Bus coupler in first slave ID of this device controllable(ID-Offset = 0)	
0x11	Bus coupler in 2nd. slave ID of this device controllable(ID-Offset = 1)	
0x12	Bus coupler in 3rd slave ID of this device controllable(ID-Offset = 2)	
0x13	Bus coupler in 4th slave ID of this device controllable(ID-Offset = 3)	
0x14	Bus coupler in 5th slave ID of this device controllable(ID-Offset = 4)	
0x15	Bus coupler in 6th slave ID of this device controllable(ID-Offset = 5)	
0x16	Bus coupler in 7th slave ID of this device controllable(ID-Offset = 6)	
0x17	Bus coupler in 8th slave ID of this device controllable(ID-Offset = 7)	

Table 7: Bus coupler control ID of this device

Data channel order
The data channels are enumerated by the order of the transmitted data out of the device. The ”data channel 1” data is output by the slave that is is directly connected to the SLO data output of the device. The data channel are enumerated from 1 to maximum 8.

Slave ID order
The slave IDs are enumerated by the sequence at initialisation of the BiSS bus. The slave ID 0 is occupied by the slave whose SLI data input is tied to ’low’ or connected to the SLI data input of the device. The slave IDs are enumerated from 0 to maximum 7.

DEFINITIONS

BANK x	Addr. 0x . . . ; bit 7:0	R
0x14, 0x18, 0x1C, 0x20, 0x25, 0x29, 0x2D, 0x31	A *BiSS* device may use up to 8 data chennel. This pointer points to the profile specific EDS part of this data channel. Also data channel with a length of 0 bit data length are described with a profile specific EDS entry.	

Table 8: Bank address for data channel x description(Profile EDS)

DLEN x	Addr. 0x . . . ; bit 7:0	R
0x15, 0x19, 0x1D, 0x21, 0x25, 0x29, 0x2D, 0x31	A *BiSS* data channel may carry 0 . . . 64 bit data. Data channel with a length of 0 bit data length a CRC is appliable. In safety applications the *BiSS* master does not check the CRC, in this case no standard CRC polynome for the crc is defined and the set of CRC bits need to be added to the count of data bits.	

Table 9: DLEN for data channel x

CPOLY x	Addr. 0x . . . ; bit 7:0	R
0x17, 0x1B, 0x1F, 0x23, 0x27, 0x2B, 0x2F, 0x33	A *BiSS* data channel is secured with a CRC. In standard applications CRC numbers are used with a length of up to 8 bit and a CRC start value of ”0”. This parameter defines which CRC polynome (bit 8:1) is applied to this data channel. A data channel with a a length of 0 bit data length no CRC is appliable. In safety applications the *BiSS* master does not check the CRC, in this case no standard CRC polynome for the crc is defined and the set of crc bits need to be added to the count of data bits.	

Table 10: CRC polynome 8:1 for data channel x

FORMAT x

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data format data channel X								
0x16, 0x1A, 0x1E, 0x22, 0x26, 0x2A, 0x2E, 0x32	Reserved				STOP	RESERVED	ALIGN	TYPE

Table 11: Register layout

Table STOP	Addr. . . . ; bit . . .	R
0x00	No stop bit before actuator data	
0x01	Stop bit before actuator data	

Table 12: Stop Bit

Table RESERVED	Addr. . . . ; bit . . .	R
0x00	Reserved	

Table 13: Reserved Bit

Table ALIGN	Addr. . . . ; bit . . .	R
0x00	Right aligned (typically multiturn and linear systems)	
0x01	Left aligned (typically singleturn systems)	

Table 14: Alignment Bit

Table TYPE	Addr. . . . ; bit . . .	R
0x00	Sensor data	
0x01	Actuator data	

Table 15: Type Bit

EDS EXAMPLE I

This example describes the EDS (common part) of an linear encoder:

- Nonius calculation
- No multi turn used
- iC-MN based
- Material measure with 512 master periods / 9 bit
- Resolution of periode 10 bit
- Total resolution 19 bit

Tolerances of the oscillator
over temperature range -40°C .. +125°C
over supply voltage range 5,V +/-10%
Condition: calibrated BIAS current 200 µA.
+/- 15%, calibrated 8 MHz system clock (125 nsec system grid)
BiSS timeout sampling with 2 MHz (500 µsec grid), depending on f_osc

Variation of internal oscillator
OSCFAKTORMIN = 85% = 0.85
OSCFAKTORMAX = 115% = 1.15

Conversion time
Conversion time each channel, used bit length
t_conv_M UBL_M = 10 bit = 3.13 µsec
t_conv_S UBL_S + SBL_S = 5 bit + 4 bit = 9 bit = 2.75 µsec
t_conv_N UBL_N + SBL_N = 4 bit + 4 bit = 8 bit = 2.5 µsec
t_processing (15 + 2) * 1/f_osc = 17 * 125 nsec = 2.125 µsec
t_BiSS_sync 3 * 1/f_osc = 3 * 125nsec = 0.375 µsec
Sum 10.88 µsec (multiples of 8 MHz) = 11 µsec
TBUSY_S = 11 µsec * OSCFAKTORMAX = 12.65 µsec (unit 250 nsec) = 12.75 µsec

Timeout
16 µsec typical
Oscillator variation + BiSS timeout sampling (4/f_osc = 4/8 MHz = 0.5 µsec
TO_MIN = 16 µsec * OSCFAKTORMIN = 13.6 µsec
TO_MAX = 16 µsec * OSCFAKTORMAX + 0.5 µsec * OSCFAKTORMAX = 18.975 µsec

Timeout_S
1 µsec typical
TOS_MIN = 1 µsec * OSCFAKTORMIN = 0.85 µsec
TOS_MAX = 1 µsec * OSCFAKTORMAX + 0.5 µsec * OSCFAKTORMAX = 1.75 µsec

EEPROM Mapping EDS USER
with C16 EEPROM possible configurations:
3-4-25 (recommended, EDS sufficient and USER DATA maximized)
3-12-17
3-24-5

3-4-25 partition:

- Bank0 CFG(1/3)
- Bank1 CFG(2/3)
- Bank2 CFG(3/3)
- Bank3 EDS common part (1/4)
- Bank4 EDS BP3 part (2/4)
- Bank5 EDS Reserved (3/4)
- Bank6 EDS Reserved (4/4)
- Bank7 USER(1/25)
- Bank8.. USER(2/25)
- Bank31 USER(25/25)

Adr.	Symbol	Description	Format	Unit	Values
0x00	EDS_VER	EDS version (continuous number)	U8	-	1
0x01	EDS_LEN	EDS length (bank count completely)	U8	Banks	2
0x02	USR_STA	Bank address USER start (bank selection in address 64)	U8	-	7
0x03	USR_END	Bank address USER end (bank selection address 64)	U8	-	15
0x04	TMA	Minimum permitted clock period on MA (TMA)	U8	1 ns	100
0x05	TO_MIN	Minimum *BiSS* timeout (0= adaptive)	U8	250 ns	54
0x06	TO_MAX	Maximum *BiSS* timeout (0= adaptive)	U8	250 ns	76
0x07	TOS_MIN	Minimum *BiSS* timeout_S (0= adaptive)	U8	25 ns	34
0x08	TOS_MAX	Maximum *BiSS* timeout_S (0= adaptive)	U8	25 ns	70
0x09	TCLK_MIN	Minimum sampling periode adaptive timeout	U8	25 ns	0
0x0A	TCLK_MAX	Maximum sampling periode adaptive timeout	U8	25 ns	0
0x0B	TCYC	Minimum cycle time (0= no limitation)	U8	250 ns	0
0x0C	TBUSY_S	Maximum processing time SCD	U8	250 ns	51
0x0D	BUSY_S	Additional processing time SCD in clocks	U8	TMA	0
0x0E 0x0F	PON_DLY	Maximum "power on delay" until control communication is available	U16[1]	1 ms	3
0x10	DC_NUM	Number of data channel in this device (number of words)	U8	-	1
0x11	SL_NUM	Area of validity for this EDS (number of slave addresses)	U8	-	1
0x12	SL_OFF	Memory location for this EDS (slave ID within this device)	U8	-	0
0x13		Reserved			0
0x14	BANK1	Bank address for content description data channel 1 (profile EDS)	U8	-	4
0x15	DLEN1	Data length data channel 1	U8	bit	20
0x16	FORMAT1	Data format data channel 1	U8	bit	0
0x17	CPOLY1	CRC polynome(8:1) for data channel 1 = 0x43(8:1) = 0x21	U8	-	0x21
0x18	BANK2	Bank address for content description data channel 2 (profile EDS)	U8	-	0

0x19	DLEN2	Data length data channel 2	U8	bit	0
0x1A	FORMAT2	Data format data channel 2	U8	bit	0
0x1B	CPOLY2	CRC polynome(8:1) for data channel 2	U8	-	0
0x1C	BANK3	Bank address for content description data channel 3 (profile EDS)	U8	-	0
0x1D	DLEN3	Data length data channel 3	U8	bit	0
0x1E	FORMAT3	Data format data channel 3	U8	bit	0
0x1F	CPOLY3	CRC polynome(8:1) for data channel 3	U8	-	0
0x20	BANK4	Bank address for content description data channel 4 (profile EDS)	U8	-	0
0x21	DLEN4	Data length data channel 4	U8	bit	0
0x22	FORMAT4	Data format data channel 4	U8	bit	0
0x23	CPOLY4	CRC polynome(8:1) for data channel 4	U8	-	0
0x24	BANK5	Bank address for content description data channel 5 (profile EDS)	U8	-	0
0x25	DLEN5	Data length data channel 5	U8	bit	0
0x26	FORMAT5	Data format data channel 5	U8	bit	0
0x27	CPOLY5	CRC polynome(8:1) for data channel 5	U8	-	0
0x28	BANK6	Bank address for content description data channel 6 (profile EDS)	U8	-	0
0x29	DLEN6	Data length data channel 6	U8	bit	0
0x2A	FORMAT6	Data format data channel 6	U8	bit	0
0x2B	CPOLY6	CRC polynome(8:1) for data channel 6	U8	-	0
0x2C	BANK7	Bank address for content description data channel 7 (profile EDS)	U8	-	0
0x2D	DLEN7	Data length data channel 7	U8	bit	0
0x2E	FORMAT7	Data format data channel 7	U8	bit	0
0x2F	CPOLY7	CRC polynome(8:1) for data channel 7	U8	-	0
0x30	BANK8	Bank address for content description data channel 8 (profile EDS)	U8	-	0
0x31	DLEN8	Data length data channel 8	U8	bit	0
0x32	FORMAT8	Data format data channel 8	U8	bit	0
0x33	CPOLY8	CRC polynome(8:1) for data channel 8	U8	-	0
0x34	BC_OFF	No bus coupler	U8	-	0
0x35		Reserved	U8	-	0
0x36		Reserved	U8	-	0
0x37		Reserved	U8	-	0
0x38		Reserved	U8	-	0
0x39		Reserved	U8	-	0
0x3A		Reserved	U8	-	0
0x3B		Reserved	U8	-	0
0x3C		Reserved	U8	-	0
0x3D		Reserved	U8	-	0
0x3E		Reserved	U8	-	0
0x3F	CHKSUM	Check sum (addition of all bytes within this bank)	U8	-	xx

Table 17: Electronic Data Sheet (allgemeiner Teil)

REVISION HISTORY

Rev	Notes	Pages affected	Details
A1	Initial version		
A2		1	BP conformitity hint not required, removed
		3	Note added: Big Endian for U16
		3	Code GRAY not available
		3	PON_DLY: maximum to 5 seconds reduced
		3	DC_NUM: minimum 0 data channel possible
		4	BC_OFF parameter in addresse 0x34, downwards compatible (0x00 = bus coupler not present)
		5	BC_OFF table added
		5	Explanation ”Data channel order” added
		5	Explanantion ”Slave ID order” added
		6	Table 11 FORMATx Bit 2 now reserved
		6	Table 13 CODE now RESERVED = 0
		7	EDS Example I added

Table 19: Revision History